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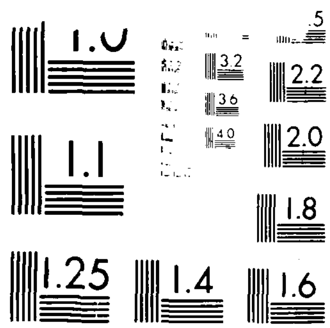
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HIGH SPEED COMPOUND SEMICONDUCTOR DEVICES IN LAYERED STRUCTURES

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Much progress has been made in the growth of GaAs on Si, GaAs MESFETs, MODFETs, HBTs, lasers on Si, modeling of MODFETs and MODFET ring oscillators, InGaAs/AlGaAs MODFETs, InGaAs hot electron transistors, GaAs/AlAs resonant tunneling transistors, single and multi quantum wells. Accomplishments were reported in about 200 journal articles, 50 conference papers and 25 seminars over the past three years. Only the GaAs on Si, $In_yGa_{1-y}As$/AlGaAs MODFET and InGaAs hot electron transistor related research accomplishments are summarized in this document. A list of publications covering all of the research funded by the AFOSR is provided as an appendix for those who are interested.

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III-V Semiconductors on Si Substrates

I. Introduction

The use of Si as a substrate material for the growth of GaAs provides several advantages and new possibilities. First, the growth of GaAs on Si would allow Si circuits to be combined with that of GaAs. In this way, the critical functions could be performed with GaAs while the less critical ones could be done in Si, taking advantage of the high integration densities. Another possibility is the use of GaAs lasers for optical off chip communication, reducing the off chip driver requirements which is at present a major bottleneck in overall system speed.

Aside from these new possibilities mentioned above, there are advantages in using Si substrates for GaAs technology itself. At present, GaAs substrates larger than 3" diameter are not available. The growth of GaAs on large diameter Si wafers would provide a larger diameter wafer on which to build GaAs ICs. Further, Si has a larger thermal conductivity than does GaAs which would allow higher power dissipation levels. Si is also much less expensive and is mechanically stronger than GaAs, minimizing wafer breakage problems.

The growth of device quality GaAs on Si poses some difficult problems to overcome. First, there is a 4% lattice mismatch between the materials. Secondly, GaAs is a polar semiconductor while Si is a nonpolar one which can give rise to defects called antiphase domains. In antiphase domains, the GaAs growth starts in some regions with the cation plane while in ot er regions with the anion plane. The growth of GaAs on Si provides an interesting system to study the mechanisms involved in the initial stages of epitaxy.

II. Growth and Materials Properties

As mentioned above, the suppression of antiphase domains is an important issue in the growth of GaAs on Si. The method we have used to suppress antiphase disorder is to grow on the (100) surface and to deposit an As prelayer to ensure a uniform starting plane across the substrate.[1,2] Since As is quite volatile, a low initial growth temperature is required. While it is possible to grow GaAs at these low temperatures by reducing the growth rate, it would be better if it were possible to use higher growth temperatures, as better quality material could be obtained.

In growing GaAs in the (100) direction, planes alternate between Ga and As, and thus by ensuring a uniform starting plane on an atomically flat substrate surface, the material should be free of antiphase disorder. If there are steps in the substrate surface however, the situation is modified. It is known that in the Si (100) surface both single and double atomic layer steps exist. At a single atomic layer step with uniform As layer coverage, an antiphase boundary will be generated. However, we have found through the use of chemical etching studies,[3] x-ray scattering,[4] Raman scattering experiments and transmission electron microscopy (TEM)[5] that the layers are free of antiphase disorder.

The second issue in the growth of GaAs on Si is the 4% lattice mismatch. TEM investigations have revealed that there are two types of edge dislocations which accommodate the majority of the mismatch in this system, one with its Bürgers vector in the plane of the substrate and one with its Bürgers vector nonparallel to the substrate plane. When the dislocation has its Bürgers vector in the substrate plane, the dislocation line cannot propagate into the epilayer and therefore does not degrade the material quality. Also, fewer

dislocations of this type are required to accommodate the mismatch. The use of the strain field of a strained layer superlattice to bend the dislocations combined with intentionally generating perfect edge dislocations propagating in the growth plane has reduced the dislocation densities dramatically.

Another issue with regard to the problem of mismatch is that GaAs and Si do not have the same thermal expansion coefficient. Studies of x-ray scattering[4] have revealed that the GaAs is expanded in the substrate plane (compressed in the growth direction) which is opposite that expected by comparing lattice constants. Since GaAs has a larger thermal expansion coefficient than Si, this would be expected, and the amount of strain roughly corresponds to that expected from the difference between growth temperature and room temperature. Studies by Raman scattering have shown no observable shift in the LO phonon peak, indicating no strain. However, the penetration depth of the light in this experiment was about 800Å, which demonstrates that the strain in these samples is confined to the interfacial region.

III. Devices and Fabrication

The properties of devices fabricated in these GaAs layers grown on Si look quite promising. We have investigated the properties of GaAs MESFETs on Si at both dc and microwave frequencies,[6] and have found very little difference (if any) between those grown on GaAs substrates and on Si substrates. Furthermore, the properties of both types were found to be nearly identical to GaAs MESFETs with the same geometry fabricated by direct implantation into GaAs substrates. Current gain cutoff frequencies and maximum oscillation frequencies of f_t=13.3GHz and f_{max}=30GHz were obtained for GaAs MESFETs with 1.2μm gate grown on Si substrates as shown in Figure 1. At dc, GaAs/AlGaAs

MODFETs on Si having characteristics nearly identical to those grown on GaAs have been obtained.[1]

Since field effect transistors are majority carrier devices, their properties are not as sensitive to the material properties as a minority carrier device. Therefore, the bipolar transistor and in particular the HBT provides a unique tool to investigate the material quality of GaAs on Si. We have already obtained HBTs with common emitter current gains of $\beta=13$ for a structure with a 0.2μm thick base.[7] This value of β is certainly a usable value from the standpoint of circuit operation, however, it is not as high as could be obtained from the same structure grown on GaAs. A series of HBT structures was grown with the base width as a parameter in order to determine whether the gain is limited by recombination in the neutral base region. For base widths of 0.2, 0.15 and 0.1μm, current gains of β=12, 13 and 12 were obtained, indicating that recombination in the neutral base region is not the limiting mechanism.

For a relatively large geometry HBT on Si ($4x20\mu m^2$ emitter), we have obtained a current gain cutoff frequency[8] of f_T=30GHz. Values of $f_{max}\cong$11.3GHz have also been obtained as shown in Figure 2. These results compare with the values of f_T=40GHz and f_{max}=26GHz which are the best reported for an HBT structure on GaAs with an emitter width of ~1.5μm.

Heterojunction devices hold significant advantages over Si devices. Therefore, the ability to monolithically integrate the two would have many advantages. A useful feature of GaAs on Si is that the typical processing temperatures are very much different and the two semiconductors are quite different chemically. We have demonstrated[9] that the processing steps involved in producing GaAs devices on Si are compatible with Si NMOS devices, by

showing that little or no degradation in NMOS FETs occurred in fabricating GaAs/AlGaAs MODFETs on the same wafer. This result demonstrates the possibility of a monolithically integrated GaAs/Si system.

IV. Conclusion

Despite the inherent difficulties in growing GaAs epitaxial layers on Si, excellent device performance has been achieved. These results open an entire new direction for heterojunction electronics as it makes possible the combination of Si devices with high speed heterojunction devices. This new direction only adds to the importance of III-V heterojunction devices in future electronics.

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Figure Captions

Figure 1. Maximum available gain and small signal current gain plotted as a function of frequency for a 1.2μm GaAs MESFET on Si.

Figure 2. Microwave gain and current gain versus frequency for a $4x20\mu m^2$ emitter GaAs/AlGaAs heterojunction bipolar transistor grown on Si.

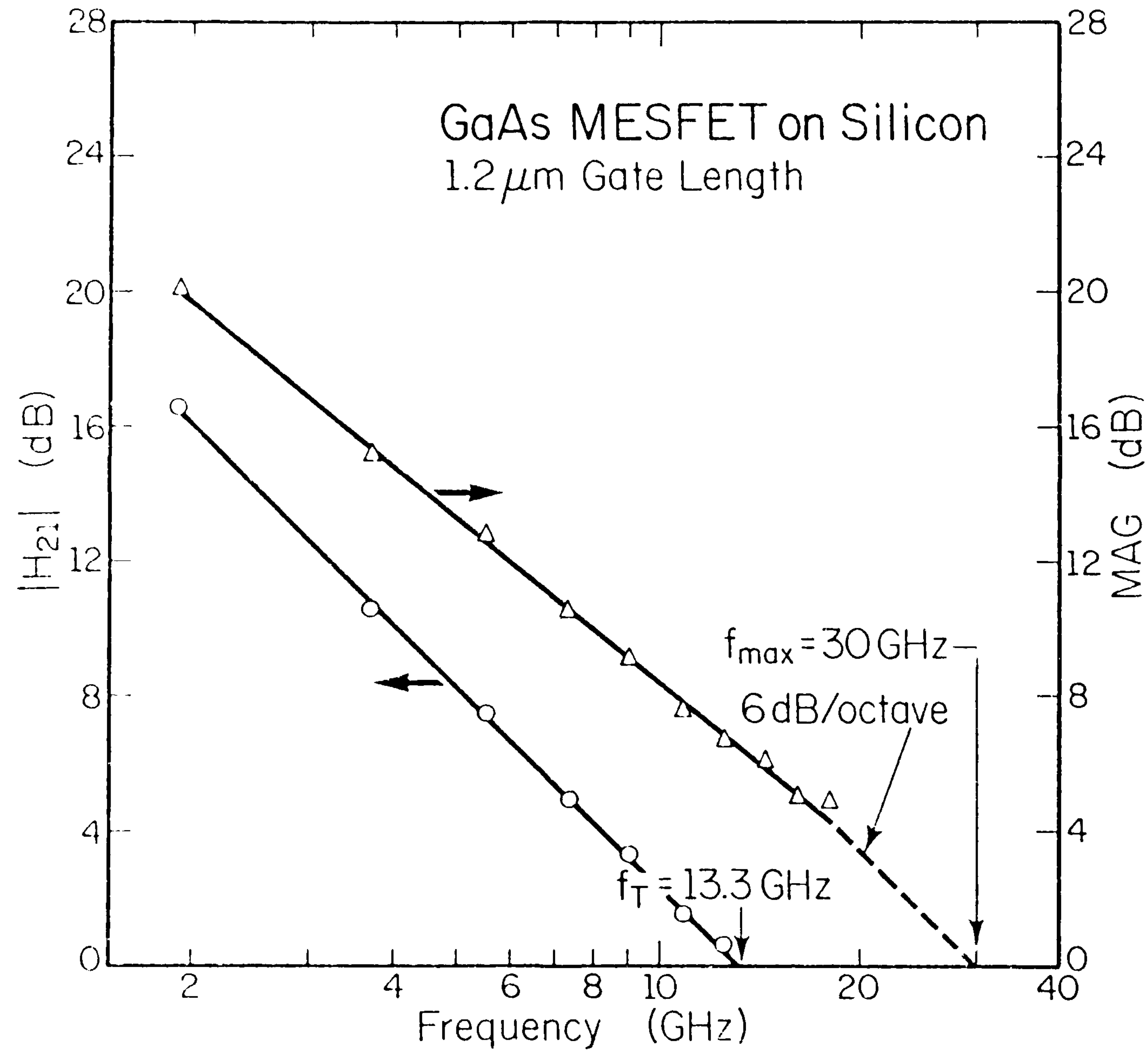
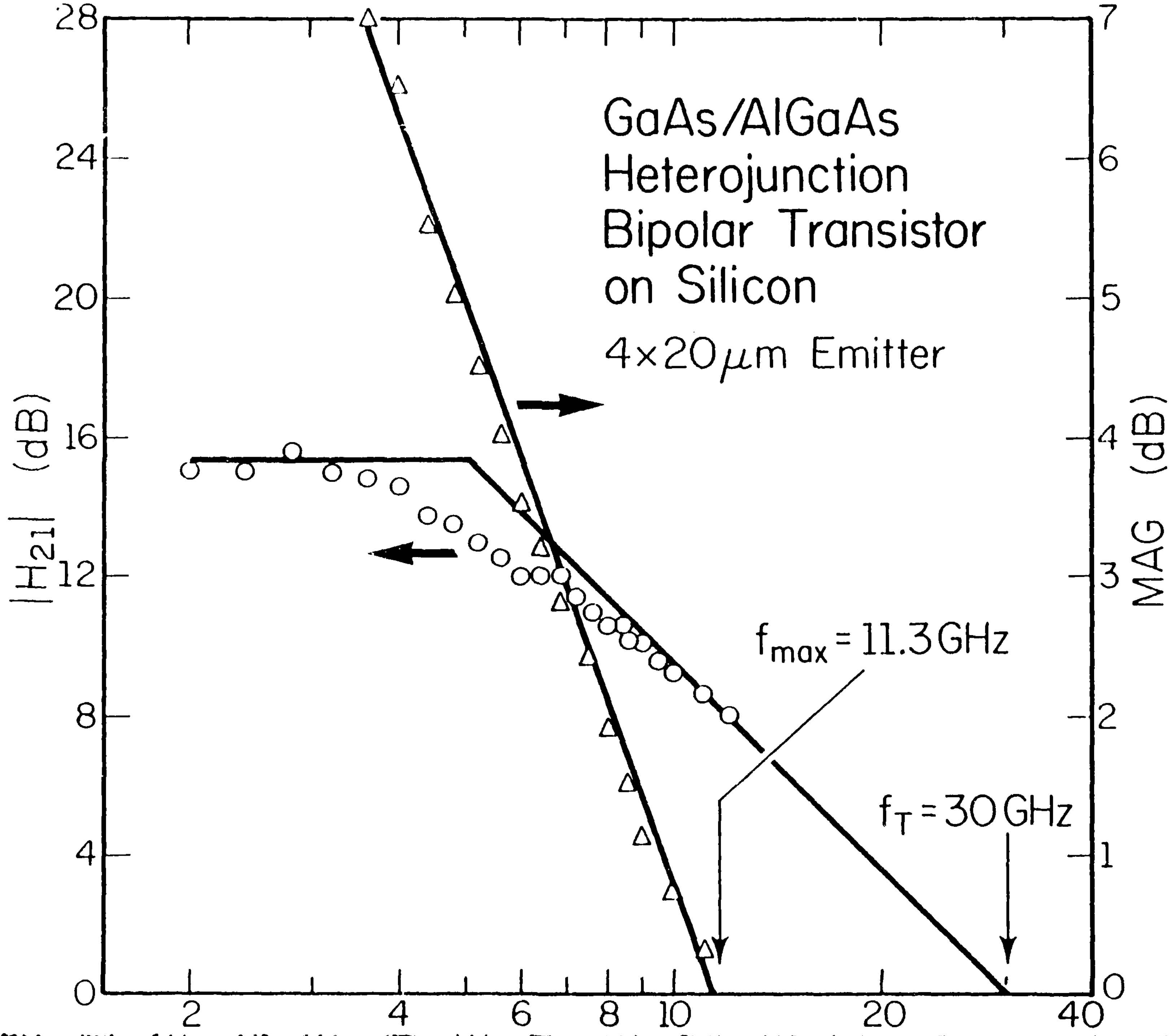

GaAs MESFET on Silicon
1.2 μm Gate Length
$|H_{21}|$ (dB)
MAG (dB)
f_{max} = 30 GHz
6 dB/octave
f_T = 13.3 GHz
Frequency (GHz)
28
24
20
16
12
8
4
0
2
4
6
8
10
20
40

Fig. 1


GaAs/AlGaAs
Heterojunction
Bipolar Transistor
on Silicon
4×20μm Emitter
f_{max} = 11.3GHz
f_T = 30GHz
$|H_{21}|$ (dB)
MAG (dB)
0
4
8
12
16
20
24
28
1
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3
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7
2
4
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8
10
20
40

Fig 3

High Performance AlGaAs/InGaAs Pseudomorphic Modulation-Doped FETs

I. Introduction

Modulation-doped heterojunction semiconductor structures have been shown to be excellent candidates for field effect transistors (MODFETs) due to their superior electron transport properties parallel to the heterointerface. Electrons from donors in the higher band-gap materials are confined in a potential well in the narrow band-gap material forming a degenerate two-dimensional electron gas (2DEG). The separation of these electrons from the ionized donors greatly reduces impurity scattering resulting in a high electron mobility and saturation velocity. By far the most commonly studied MODFET is based on the GaAs/(Al,Ga)As system although other systems such as InGaAs/InP and InGaAs/AlInAs have also been demonstrated. Recently a new type of MODFET called the pseudomorphic or strained-quantum-well MODFET using the InGaAs/GaAs system has been introduced. A thin layer of the narrow band-gap InGaAs, which is lattice mismatched to GaAs (~1%), is sandwiched between an undoped GaAs buffer and a doped GaAs cap layer. The InGaAs is thin enough (~200Å) that the lattice strain is taken up coherently by this quantum well resulting in a dislocation-free "pseudomorphic" material. More recently we demonstrated that by replacing the GaAs with the even higher band-gap low mole fraction AlGaAs that device performance rivaling the best reported GaAs/AlGaAs MODFET results are possible.[1-4] In this section we describe the advantages of this system over the GaAs/AlGaAs system; these advantages include improved noise performance, higher operational frequencies and no degradation during cryogenic operation.

An important consideration with any modulation-doped system is the conduction band discontinuity (ΔE_c) or, more importantly, the discontinuity between the donor level in the high band-gap material and the narrow bandgap conduction band. A small discontinuity results in less efficient electron transfer and therefore a smaller 2DEG concentration. Furthermore, a small ΔE_c compounds the problems of the parasitic MESFET effect and may increase the possibility of hot electron injection into the higher band-gap material. In the GaAs/$Al_xGa_{1-x}As$ system an aluminum mole fraction greater than 0.2 is needed to provide a sufficiently large ΔE_c for adequate electron transfer; in the InGaAs/$Al_xGa_{1-x}As$ system a mole fraction of only about x=0.15 appears sufficient because the conduction band of InGaAs lies below that of GaAs. The use of high mole fraction $Al_xGa_{1-x}As$ ($x \gtrsim 0.2$), however, can lead to persistent photoconductivity (PPC) effects. These include the 'collapse' of drain I-V characteristics (see Fig. 1a) and uncontrollable threshold voltage shifts at 77K (see Fig. 1b). This latter problem of threshold voltage shifts occurs even in devices which do not show the collapse and make 77K logic very unreliable. Deep levels (DX centers) in the $Al_xGa_{1-x}As$ are believed to be the cause of the persistent properties. The InGaAs/AlGaAs MODFET avoids these problems by using a lower mole fraction ($x \lesssim 0.2$) where the DX occupation probability is significantly reduced.

In micron and submicron structures the intrinsic transconductance is (to first order) determined by the product of the average electron velocity and the 2DEG capacitance. A higher transconductance is expected with the InGaAs based systems over GaAs due to the higher saturation velocity in InGaAs. The 2DEG capacitance can likewise be made higher by decreasing the thickness and increasing the doping concentration of the higher band-gap material. The

InGaAs/AlGaAs system has the advantage over GaAs/AlGaAs that higher doping densities are possible with low mole fraction $Al_xGa_{1-x}As$ due to reduced donor compensation. Furthermore, the AlGaAs trap density, which is in part proportional to the doping concentration is significantly reduced in low mole fraction $Al_xGa_{1-x}As$.

The same advantages of InGaAs/AlGaAs over GaAs/AlGaAs MODFETs in dc performance can be applicable to microwave performance. Consider the limiting current gain cut-off frequency given by $f_T = v_a/2\pi L'_g$ where v_a is the average electron velocity under the gate and L'_g is the gate length. The improved electron saturation velocity in InGaAs should result in a significant increase in f_T compared with that of GaAs FETs. Generation-recombination noise is also expected to be lower due to reduction of occupied deep levels in low mole fraction $Al_xGa_{1-x}As$.

II. Device Structure and Fabrication

The pseudomorphic single quantum well InGaAs/AlGaAs structures studied were grown by MBE on semi-insulating GaAs substrates. Figure 2(a) shows a typical structure which begins with a ten period superlattice (not shown) consisting of 50Å GaAs and 20Å AlAs layers. This is followed by an unintentionally doped 1μm GaAs buffer layer and either a 150 or 200Å quantum-well of (strained) undoped $In_yGa_{1-y}As$ with y varying from 0.05 to 0.2. Finally a 30Å $Al_{0.15}Ga_{0.85}As$ undoped set-back layer, 350Å n-$Al_{0.15}Ga_{0.85}As$ doped $3\times10^{18}cm^{-3}$ with Si, and, a 200Å n^+-GaAs cap layer to facilitate ohmic contact formation is grown. The band diagram of a typical pseudomorphic structure is shown in Fig. 2(b).

Device fabrication is in no way different from that used with the well-established GaAs/AlGaAs system. The process begins with defining and etching of mesa isolation patterns using standard UV photolithographic and etching techniques. Source and drain regions are then defined in positive photoresist and AuGe/Ni/Au contacts evaporated. The metal is lifted-off and alloyed at 500°C in hydrogen atmosphere. Nominal 1μm gate patterns in 3μm channels are defined using chlorobenzene treated photoresist (AZ4110). Next a wet chemical etch is used to recess the gate region below the GaAs cap layer; this step is immediately followed by evaporation of ~3000Å of aluminum. Finally a thick Ti/Au overlay metallization is deposited forming bond pads. A unoptimized 1 x 290μm T-gate FET structure is used for microwave characterization and half a 1x290μm T-gate FET (145μm) is used for dc characterization. Fabricated wafers are scribed into individual devices and typical FETs bonded to TO-18 headers for dc measurements. S-parameter measurements were made up to 26.5 GHz at Cascade Microtech, Inc. using an on-wafer microwave prober.

III. DC Characterization

Hall measurements performed on the sample shown in Fig. 2 indicate a 300K low field mobility and areal concentration of $6000 cm^2/V\text{-}s$ (lowered by parallel conduction) and $1.4 \times 10^{12} cm^{-2}$ respectively; at 77K, these values are $29{,}000 cm^2/V\text{-}s$ and $1.2 \times 10^{12} cm^{-2}$ and exhibited no PPC effect. This large sheet carrier concentration is certainly adequate for high current FETs. When a 100Å $Al_{0.15}Ga_{0.85}As$ set-back was substituted for the 30Å layer the 2DEG concentration reduced to $3 \times 10^{11} cm^{-3}$ and the Hall mobility increased to 8,000, 95,000 and 158,000 $cm^2/V\text{-}s$ at 300K, 77K and 10K, respectively which represent the highest yet reported mobilities for a strained-layer structure. The low sheet carrier concentration, however, makes this higher-mobility structure

less suitable for FETs.

To demonstrate the cryogenic performance of InGaAs/AlGaAs pseudomorphic modulation-doped material is superior to that of the more conventional GaAs/GaAs material, Hall measurements were made down to 12K in the light and dark. At 12 and 77K measurements of persistent photoconductivity were performed by measuring the sample in the dark just following illumination. As Fig. 3 shows there is virtually no change in either the mobility or sheet carrier concentration between light and dark for the InGaAs/GaAs sample as compared to a conventional GaAs/AlGaAs sample of similar structure. These data show that for similar carrier concentrations the larger mole fraction ($x=0.3$) necessary in the GaAs/AlGaAs system results in significant light sensitivity and PPC effects.

Devices were dc characterized using an HP4145 semiconductor parameter analyzer at both 300 and 77K. The current-voltage and FET transfer characteristics at 300K are shown in Fig. 4(a) and (b), respectively, for the 1x145μm pseudomorphic structure given in Fig. 2(a). The curves show excellent saturation and pinch-off characteristics with an output conductance of 700μS and an on resistance of 18.4Ω. A threshold voltage, defined by a linear extrapolation of the drain current versus gate voltage to zero current, of -0.3V is measured. A peak extrinsic transconductance for this 15% In mole fraction device of 270 mS/mm at 300K is obtained at a gate voltage of +0.1V and a drain current density of 100 mA/mm. When the indium mole fraction was increased to 20% and the strained-quantum well size reduced to 150Å the (extrinsic) transconductance climbed to 310 mS/mm at 300K. This transconductance is superior to the best reported transconductances for 1um non-self-aligned GaAs/AlGaAs MODFETs. A theoretical calculation of the 15% indium FET

transfer characteristic based on a classical one-dimensional charge control model indicates a maximum intrinsic transconductance of 370 mS/mm.

Fig. 5 (a) and (b) show the 77K dc characteristics for the y=0.15 device in the dark. There is no 'collapse' as is sometimes seen in GaAs/Al$_x$Ga$_{1-x}$As MODFETs using x≥0.25. When the device is illuminated, the curves remain virtually unchanged and completely return to their original values when the source of illumination is removed. Similar characteristics were observed for other indium mole fractions. Again the saturation is extremely sharp with an output conductance of only 200μS and an on resistance of 10.9Ω. The threshold voltage at 77K increased to -0.2V representing a shift of only about 0.1V from 300K. The peak transconductance increased to 360 mS/mm at a gate voltage of +0.2V and a current density of 125 mA/mm. The 20% indium mole fraction device again showed the highest transconductance with 380 mS/mm at 77K. Table I summarizes the effect of mole fraction on transconductance. The trend of increased transconductance with y is clearly evident with the exception of the 10% which showed a reduce transconductance due to under-etching of gate recess.

A large current swing is just as important as high transconductance for logic devices where gate capacitance charging time determines switching speed. At 1V on the gate, drain currents in excess of 290 mA/mm at 300K and 310 mA/mm at 77K were obtained. This demonstrates that significant current levels are possible with the InGaAs/AlGaAs heterojunction system.

An important problem with conventional GaAs/AlGaAs MODFETs is the positive shift in threshold voltage after a gate bias sufficient to fully turn-on the channel is applied. This device instability due to bias stress appears as a hysteresis in the FET transfer characteristics. A large positive gate

voltage bends the conduction band in the (Al,Ga)As enough to allow energetic electrons to fill DX traps. The injected charge acts to decrease the 2DEG concentration and therefore shifts the transfer characteristic towards higher gate voltages. (Similar effects have been reported for Si/SiO_2 MOSFETs.) While both bias stress threshold shifts and I-V 'collapse' are measures for the quality of AlGaAs, in particular the DX occupation probability, many samples exhibiting no 'collapse' show significant threshold shifts when stressed. The bias stress test is therefore a more sensitive indicator of AlGaAs trapping problems.

Figure 6 shows the transfer characteristic before and after bias stress for both a pseudomorphic $In_{0.15}Ga_{0.85}As/Al_{0.15}Ga_{0.85}As$ and a conventional $GaAs/Al_{0.3}Ga_{0.7}As$ MODFET with similar threshold voltage and doping concentration. Measurements were performed at 77K where the trap emptying time (order of minutes) is much longer than the measurement time (~5 s). Devices were cooled to 77K with V_{DS}=2V and $V_G<V_{TH}$. A HP4140 pico-ammeter was used to monitor the drain current while the gate voltage was swept to V_G=1V, maintained for one minute, and swept back down to $V_G<V_{TH}$. Fig. 7 clearly indicates that the pseudomorphic MODFET shows virtually no threshold shift while the conventional MODFET shows a 0.12V shift. This lack of threshold shift can be attributed to low mole fraction $Al_{0.15}Ga_{0.85}As$ where the percentage of occupied DX centers is significantly reduced because of the increase in equilibrium energy of DX centers over the Fermi energy. This bias stability is especially important for practical cryogenic device operation.

The source resistance, which is a combination of the ohmic contact resistance R_c and the parasitic semiconductor resistance R_{SH}, was measured using transmission-line measurements at both 300 and 77K. The contact resistance

was measured at low electric fields where a constant 2DEG concentration could be assumed for the various gap lengths and resulted in an excellent linear fit of total resistance as a function of contact spacing. Contact resistances of 0.17Ω·mm and 0.23Ω·mm were obtained at 300 and 77K, respectively. The discrepancy between the two temperatures may be because the room te:perature contact resistance is not due solely to the contact made to the 2DEG (as is the case at 77K), but includes in parallel a better contact to the partially conducting AlGaAs.

The parasitic semiconductor resistance between the source and gate was determined at both 300 and 77K as a function of current density for current densities of 0 to 200 mA/mm. At 77K this value rises from about 165Ω/ at low current levels to 280Ω/ at 200mA/mm. This increase in resistance is due to the mobility becoming smaller as the electric field is increased. At 300K this increase is not as dramatic. The total source resistance was determined then for the relevant current density by adding the contact resistance and the product of sheet resistivity and source-gate spacing. Typical values for a 3μm source gate spacing were 2.7 and 1.0Ωmm at 300 and 77K, respectively, and are expected to improve with processing development.

The intrinsic transconductance $g_{m,\,int}$ was calculated for each gate length device (L_G=2,4,6, and 10μm) through the relation

$$g_{m,\,int}=\frac{g_m}{1-R_s\cdot g_m} \tag{1}$$

where R_s is the total source resistance discussed above and g_m is the extrinsic transconductance. The 1μm gate length device was not included because it is a part of a different mask set and was therefore processed separately. An analytic model [23] indicates that transconductance per unit gate width should

be related to gate length through the relation

$$\frac{1}{g_{m,\,int}} = \frac{1}{C_o v_{sat}} + \frac{L'_g}{2C_o \mu_o I_{Dsat}} \qquad (2)$$

where C_o is the 2DEG capacitance per unit area (assumed to be constant), v_{sat} is the 2DEG saturation velocity, μ_o is the zero-field 2DEG mobility and I_{Dsat} is the drain-current per unit length at the given gate bias. Figure 7 shows $\frac{1}{g_{m,\,int}}$ as a function of $\frac{L'_g}{I_{Dsat}}$ at both 77 and 300K. According to (2) above, the intercept at $\frac{L'_g}{I_{Dsat}}=0$ gives $\frac{1}{g_{m,\,int}(max)}$ which is equal to $\frac{1}{C_o v_{sat}}$. Good fits were obtained to eqn (2) at 300 and 77K and from the slope of the curves the zero-field 2DEG mobility was found to agree with Hall measurements. The saturation velocity, calculated from the intercept at 77K is $3.1\text{x}10^7$cm/s which is substantially higher than the average velocity of $1.7\text{x}10^7$cm/s for a 1μm gate length device determined from the relation $v_{ave}=\frac{g_{mi}}{C_o}$. Both saturation and average velocities in this system are significantly higher than those found in conventional AlGaAs/GaAs MODFETs of the same geometry.

IV. Microwave Performance

The microwave performance of pseudomorphic MODFETs were measured from 1 to 26.5 GHz using a Cascade Microtech on-wafer prober and automated network analyzer. The current gain h_{21} of the devices were determined from the measured S-parameters. Shown in Figure 8, the f_T of the 20% device is 24.5GHz, which is vastly superior to conventional MODFETs. The equivalent circuit model of Figure 9 was found to provide an excellent fit to the measured s-parameter data. Element values, listed in Table II, were fit to the data

using a least-squares-error optimization routine. Figure 8 also shows the current and power gain performance as predicted from the model. f_{max} is predicted to be 40GHz from both the circuit model and by extrapolating the power gain data at a slope of -6dB per octave; a 30% performance gain over conventional MODFETs. Table II shows element values, f_T and f_{max} for devices with increasing indium mole fractions. These results, also depicted in Figure 10, show microwave performance improves with increasing indium mole fraction. We project f_T for 1/4μm gate-length devices to exceed 100 GHz which would be 25% better than the best results reported to date.

Both high frequency and low frequency noise measurements have been performed and compared to those obtained in GaAs/AlGaAs conventional MODFETs with identical geometry. The high frequency results indicate that the noise measure at room temperature of these InGaAs/AlGaAs MODFETs are 35% lower than in otherwise identical GaAs/AlGaAs MODFETs; at 15K the noise measure is reduced by more than 50% (from that of GaAs/AlGaAs MODFETs). The projected performance for 1/4μm gate-length devices of this type is superior to anything available today.

Equivalent low frequency gate noise voltage spectra of 1μm gate-length modulation-doped FETs with $In_{0.15}Ga_{0.85}As$ quantum well structure have been measured for the frequency range of 0.01 Hz and 100 MHz and compared with the noise spectra of conventional AlGaAs/GaAs MODFETs and GaAs MESFETs. The prominent g-r noise bulge commonly observed in the vicinity of 10 KHz in the conventional MODFETs at 300K does not appear in the case of the new InGaAs quantum well MODFET. Instead, tis noise spectra indicate the presence of low intensity multiple g-r noise components superimposed on a reduced 1/f noise. The LF noise intensity in the new device appears to be the lowest amongst we

have observed in any MODFETs and MESFETs. The noise spectra at 82 K in the new device represent nearly true 1/f noise. The unusual low-noise behavior of the new structure suggests the effectiveness of electron confinement in the quantum well that significantly reduces electron trapping in the n-AlGaAs and thus, eliminates the g-r noise bulge observed in the conventional MODFETs. Both the low and high frequency noise performance of these devices are important and indicate that the InGaAs/AlGaAs pseudomorphic MODFET is an excellent candidate for low-noise millimeter wave applications.

VI. Conclusion

InGaAs/AlGaAs pseudomorphic MODFETs have been fabricated which exhibit superior dc and rf performance. Hall mobilities as high as 158,000cm^2/Vs at 10K and sheet carrier concentrations of 1.2×10^{12}cm^{-2} at 77K have been obtained on such pseudomorphic structures without exhibiting significant light sensitivity or persistent photoconductivity effects. Electron saturation velocities were found to be 20% higher than conventional GaAs/AlGaAs MODFETs.

Extremely high transconductances as high as 310 mS/mm at 300K and 380 mS/mm at 77K for devices with a 1μm gate were obtained. The pseudomorphic MODFETs exhibited none of the persistent trapping effects observed in conventional GaAs/AlGaAs MODFETs at 77K. In particular no collapse of drain I-V characteristics, minimal threshold shift from 300 to 77K, and negligible effects of gate bias stress were detected. This greatly improved cryogenic performance is attributed to the low mole fraction of $Al_{0.15}Ga_{0.85}As$ used and better carrier confinement in the InGaAs quantum well.

Microwave measurements also indicate the superiority of these devices. A maximum frequency of oscillation of 40GHz, 30% better than conventional MOD-

FETs of similar structures, and a current gain cut-off frequency of 24.5GHz, 100% better, were measured for y=0.20. Both of these frequencies were found to increase as the indium mole fraction was varied from y=0.05 to 0.2. Low-frequency noise measurements show that the noise is greatly reduced and represents nearly true the 1/f noise, and g-r noise is also drastically reduced. High frequency (8GHz) noise measurements indicate noise performance superior to conventional GaAs/AlGaAs MODFETs. These outstanding microwave characteristics and cryogenic stability make these devices very promising for high-speed logic and microwave applications.

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Figure Captions

Fig. 1. Two common problems encountered with cryogenic operation of conventional GaAs/AlGaAs MODFETs:

(a) 'Collapse of the drain I-V characteristics, and

(b) Threshold shifts resulting from gate bias.

Fig. 2. (a) Typical structure for MBE-grown InGaAs/AlGaAs pseudomorphic MODFET and

(b) the associated conduction band diagram. The conducting channel forms a two-dimensional electron gas in the strained-layer InGaAs quantum well.

Fig. 3. Hall mobility and sheet carrier concentration as a function of temperature for the conventional GaAs/$Al_{0.3}Ga_{0.7}As$ and pseudomorphic $In_{0.15}Ga_{0.85}As/Al_{0.15}Ga_{0.85}As$ MODFET structure. The pseudomorphic structure exhibits virtually no light sensitivity or PPC effects due to the lower mole fraction $Al_xGa_{1-x}As$ used.

Fig. 4. 300K current-voltage characteristics (a) and transfer characteristics (b) for 1x145μm pseudomorphic MODFET. Excellent pinchoff and saturation behavior are evident with a peak transconductance of 270 mS/mm and a maximum current density of 290 mA/mm at V_{DS}=2V.

Fig. 5. 77K Current-voltage characteristics (a) and transfer characteristics (b) for a pseudomorphic MODFET with a 3μm source-drain spacing. The gate potential ranges from -0.3V (bottom curve) to +0.9V (top curve). The I-V curves remain virtually unchanged under illumina-

tion with no PPC effects or drain I-V 'collapse'. The peak extrinsic transconductance is 360mS/mm with a maximum current of 310 mA/mm.

Fig. 6. Gate bias stress measurements for conventional $GaAs/Al_{0.3}Ga_{0.7}As$ (dashed line) and pseudomorphic $In_{0.15}Ga_{0.85}As/Al_{0.15}Ga_{0.85}As$ (solid line) MODFETs at 77K. Threshold voltage shift is due to electron trapping in the AlGaAs and is a measure of the quality of the material. The pseudomorphic MODFET shows very little shift due to the reduced trap occupation probability of low mole fraction $Al_{0.15}Ga_{0.85}As$.

Fig. 7. Dependence of gate length and intrinsic transconductance according to eqn (2).

Fig. 8. Maximum available gain (G_{max}) and short circuit current gain ($20\log|h_{21}|$) of $In_{0.20}Ga_{0.80}As/Al_{0.15}Ga_{0.85}As$ MODFET.

Fig. 9. Equivalent circuit model for MODFETs.

Fig. 10. f_T and f_{max} as functions of In mole fraction, y, for 1μm gate lengt MODFETs.

Table I. Effect of indium mole fraction on dc transconductance

y	300K		77K	
%In	$g_{m\,ext}$ (mS/mm)	V_{TH} (V)	$g_{m\,ext}$ (mS/mm)	V_{TH} (V)
5	253	-0.24	303	-0.13
10	234	-0.99	276	-1.03
15	270	-0.33	360	-0.19
20	310	-0.32	380	-0.27

Table II. Equivalent circuit parameters for devices with increasing indium mole fractions.

Parameter	Device					Unit
Indium	0	5	10	15	20	%
V_{ds}	2.5	2.5	2.5	2.5	2.5	Volts
V_{gs}	0.0	0.0	-0.4	0.0	0.0	Volts
I_d	43.0	37.0	23.0	45.0	24.0	mA
g_{mo}	42.75	80.80	76.72	77.94	81.01	mS
C_{gs}	0.54	0.69	0.67	0.58	0.53	pF
τ_t	3.26	3.87	4.38	4.23	3.90	psec
C_{dg}	29.28	21.19	43.94	32.82	35.84	fF
C_{ds}	50.29	63.87	61.13	62.62	62.76	fF
G_{ds}	2.51	4.00	2.51	2.87	2.82	mS
R_i	1.04	1.20	1.16	1.20	1.20	Ω
R_g	4.82	5.67	5.79	7.05	7.31	Ω
R_d	7.80	7.26	6.66	6.49	6.40	Ω
R_s	1.95	3.09	3.53	3.39	3.39	Ω
L_g	26.57	26.29	27.97	22.88	22.82	pH
L_d	48.47	49.49	40.28	35.16	34.90	pH
L_s	10.05	13.58	10.45	10.36	10.45	pH
f_{max}	30.5	36.0	34.5	37.0	40.0	GHz
f_T	12.0	19.0	18.5	21.5	24.5	GHz
ERF	0.013	0.018	0.017	0.019	0.016	

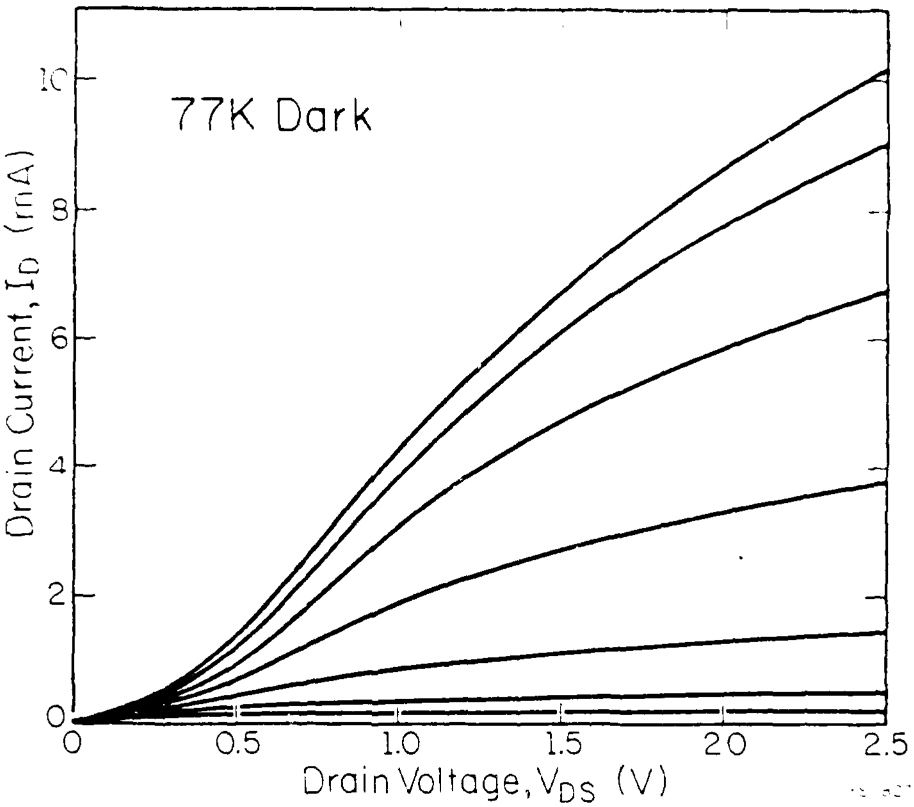
Table III. Noise Performance of $In_{0.15}Ga_{0.85}As/Al_{0.15}Ga_{0.85}As$ device, at 8GHz

T=270°K

V_d (V)	2.5	2.5	2.5
I_d (mA)	5	10	15
Associated Gain (dB)	9.5	10.5	10.9
Min. Noise Figure (dB)	3.14	3.33	3.58

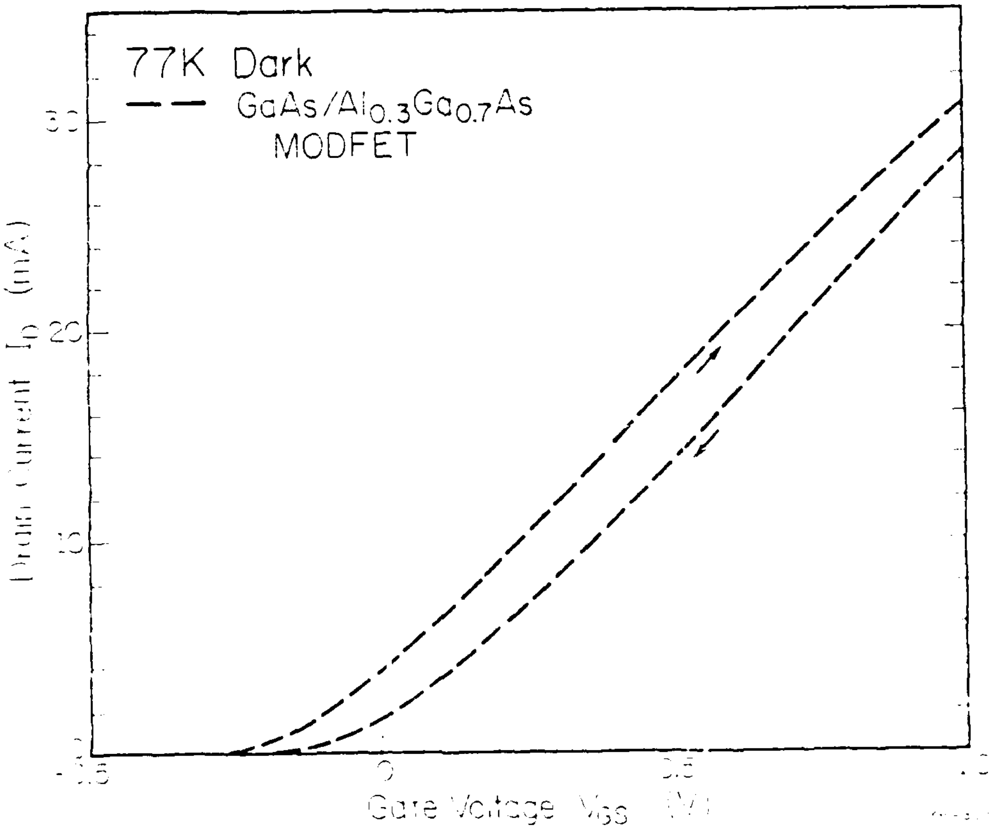
T=15°K

V_d (V)	2.5	2.5	2.5
I_d (mA)	3	5	9
Associated Gain (dB)	9.5	10.4	11.0
Min. Noise Figure (dB)	0.63	0.56	0.56



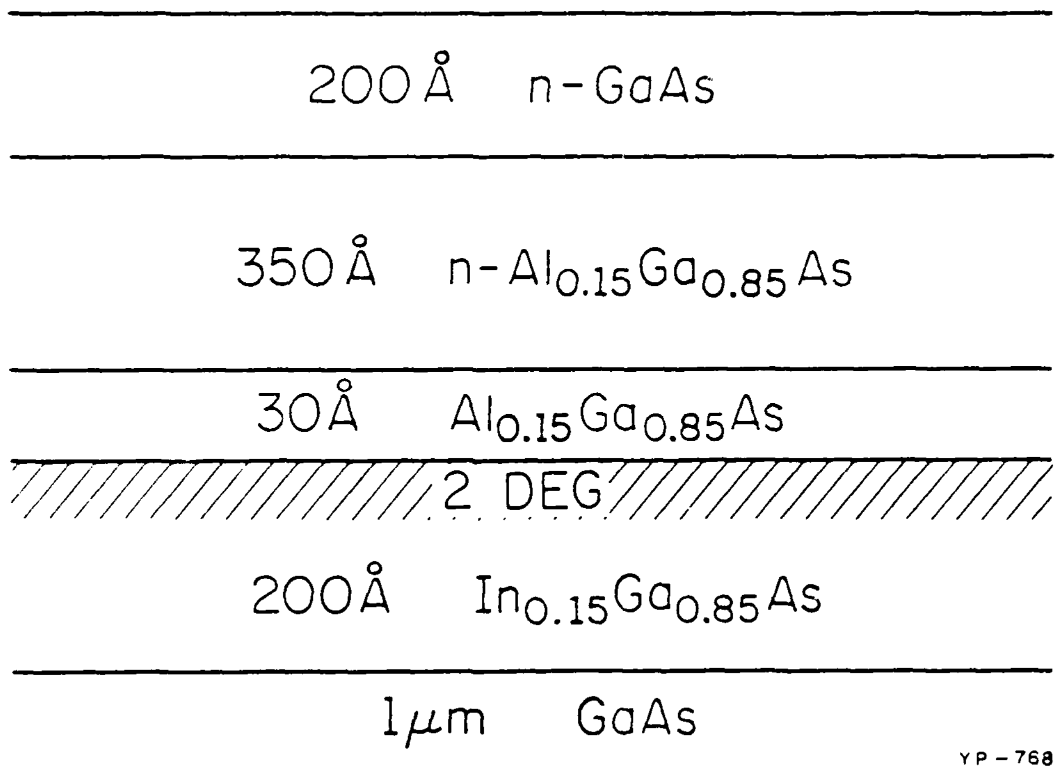
77K Dark
Drain Current, I_D (mA)
Drain Voltage, V_{DS} (V)

(a)



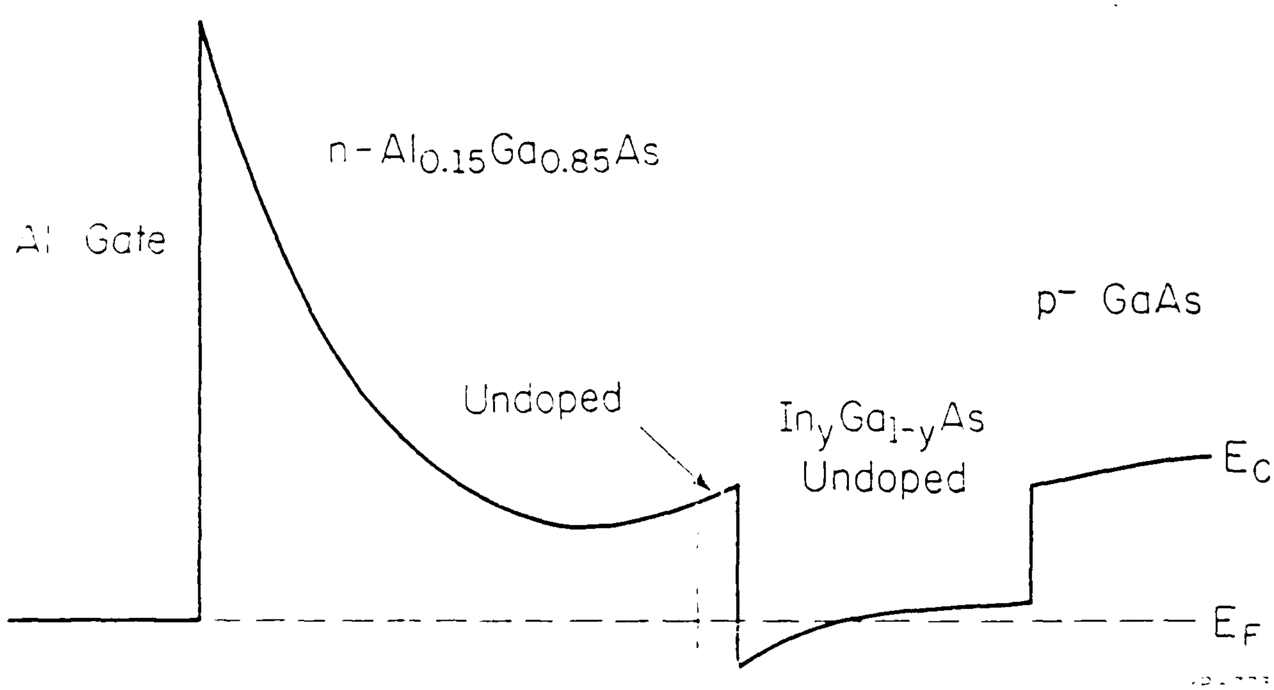
77K Dark
GaAs/$Al_{0.3}Ga_{0.7}As$
MODFET
Drain Current I_D (mA)
Gate Voltage V_{GS} (V)

(b)



200 Å n-GaAs
350 Å n-Al0.15Ga0.85As
30 Å Al0.15Ga0.85As
2 DEG
200 Å In0.15Ga0.85As
1 μm GaAs
YP - 768

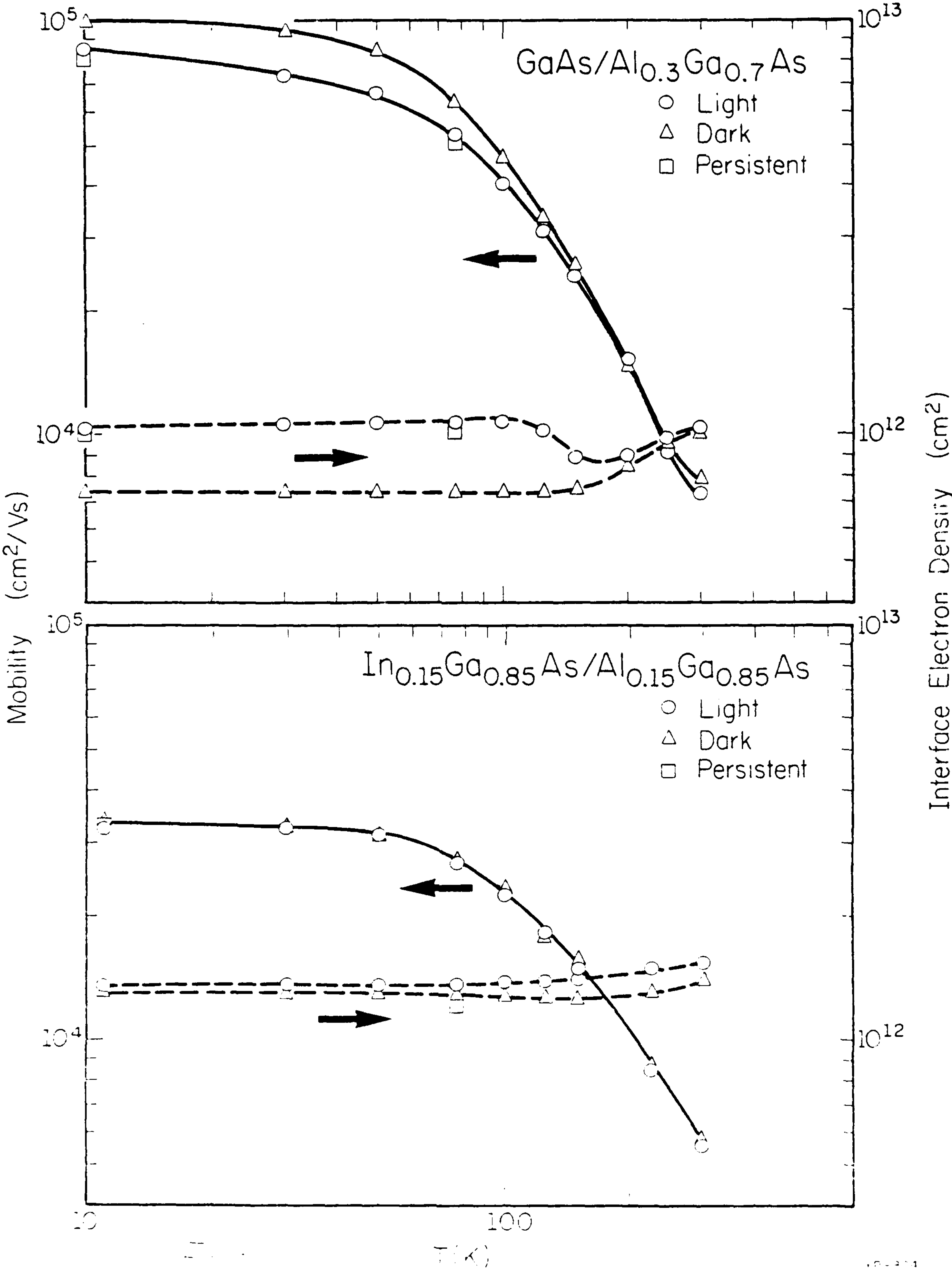
(a)



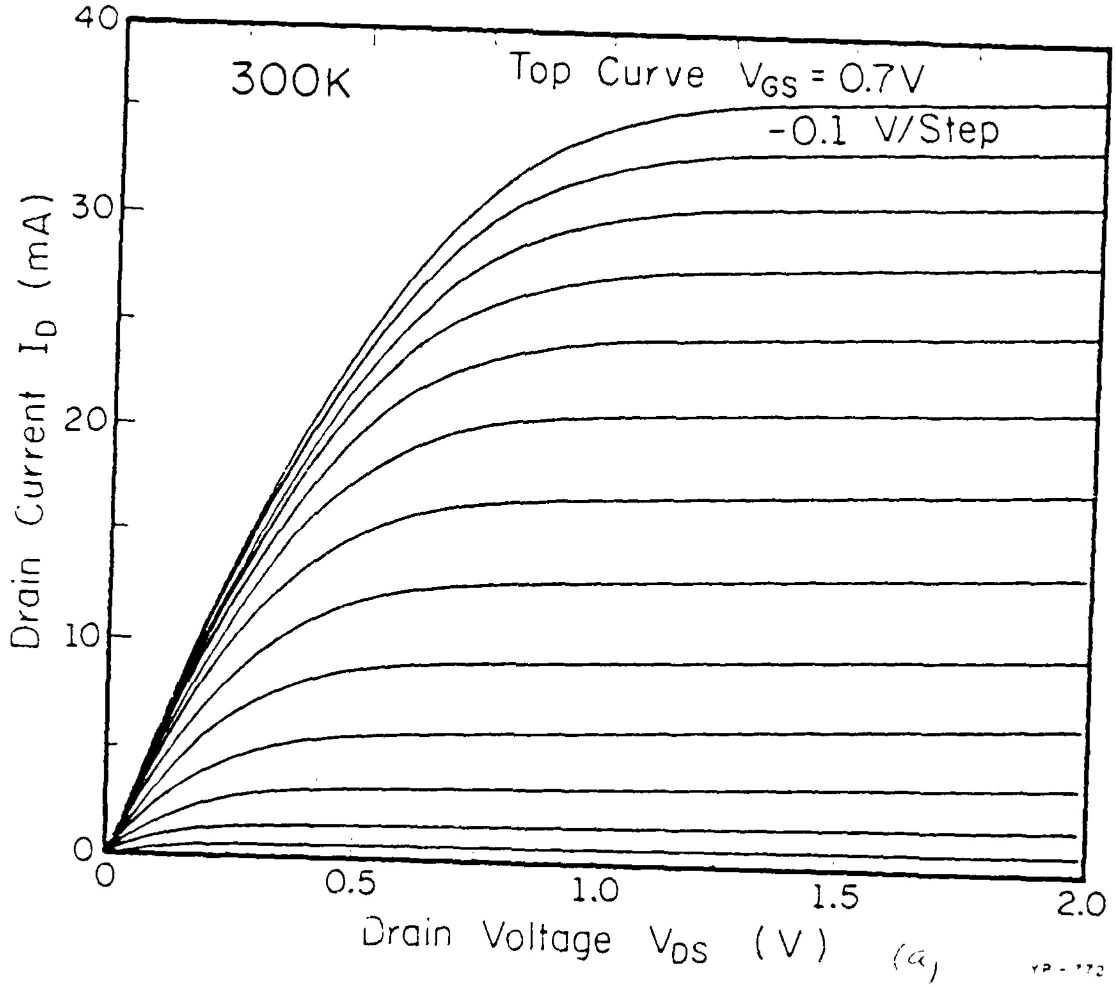
n-Al0.15Ga0.85As
Al Gate
p⁻ GaAs
Undoped
InyGa1-yAs
Undoped
Ec
EF

(b)

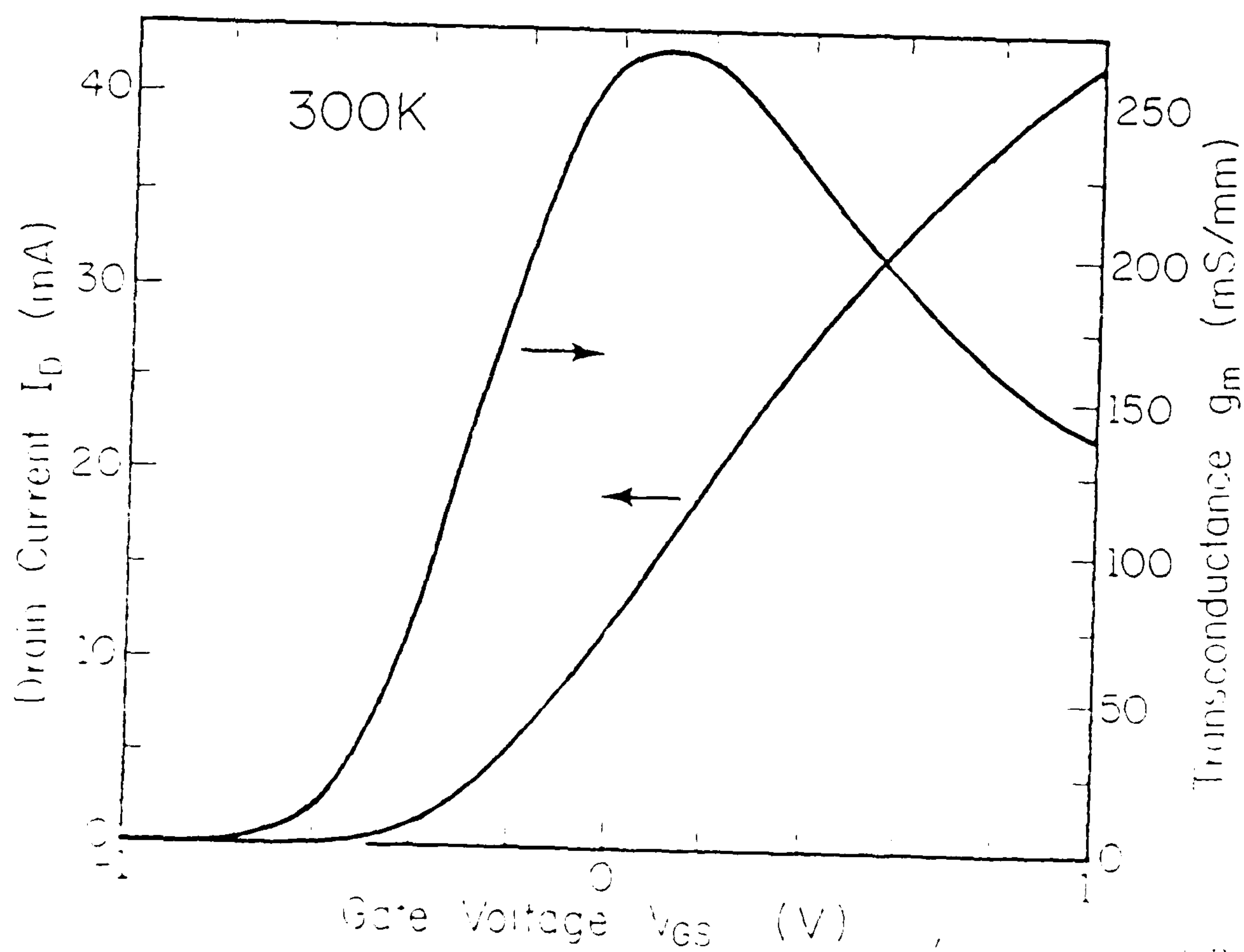
F. 2



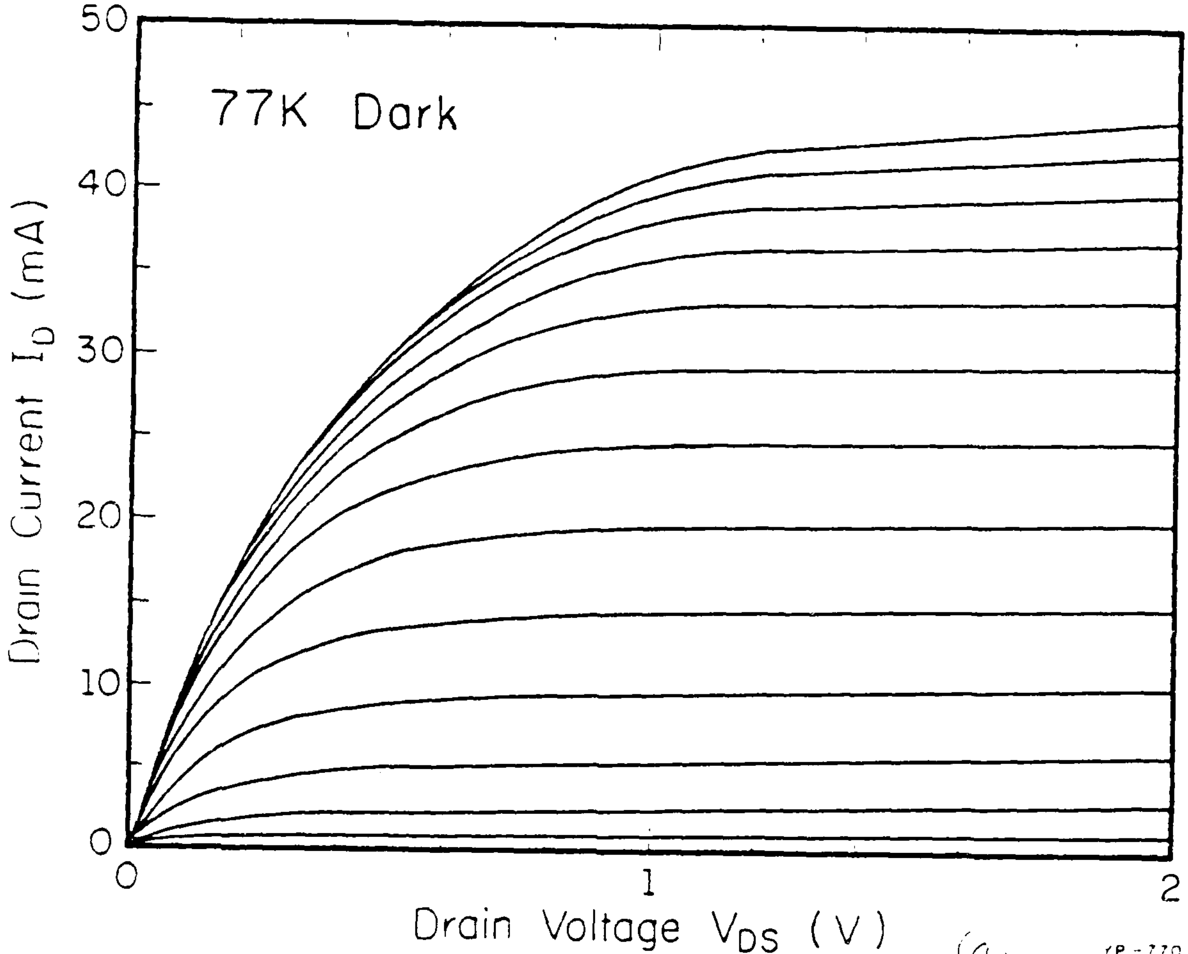
10^5
10^{13}
$GaAs/Al_{0.3}Ga_{0.7}As$
○ Light
△ Dark
□ Persistent
10^4
10^{12}
10^5
10^{13}
$In_{0.15}Ga_{0.85}As/Al_{0.15}Ga_{0.85}As$
○ Light
△ Dark
□ Persistent
10^4
10^{12}
100
Mobility (cm^2/Vs)
Interface Electron Density (cm^2)



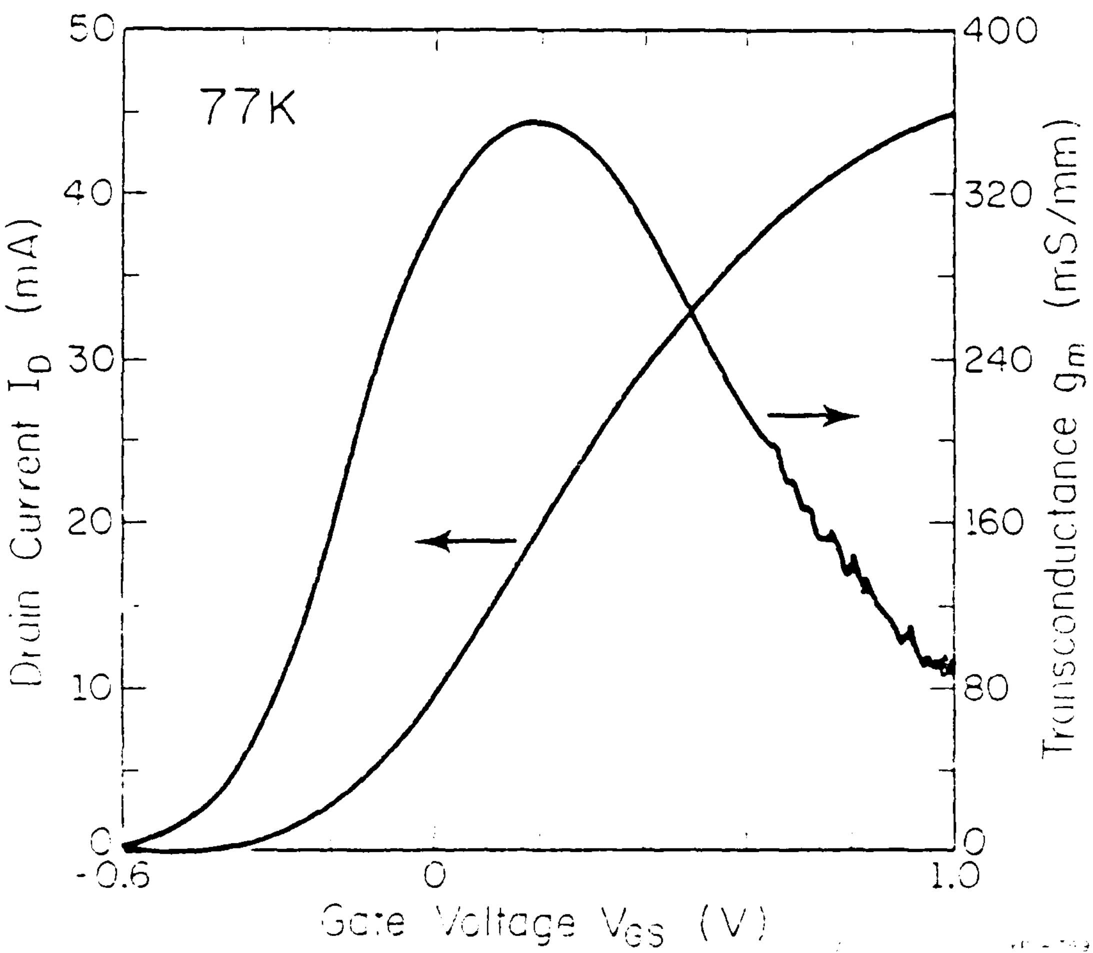
300K
Top Curve V_{GS} = 0.7V
-0.1 V/Step
Drain Current I_D (mA)
Drain Voltage V_{DS} (V)
(a)

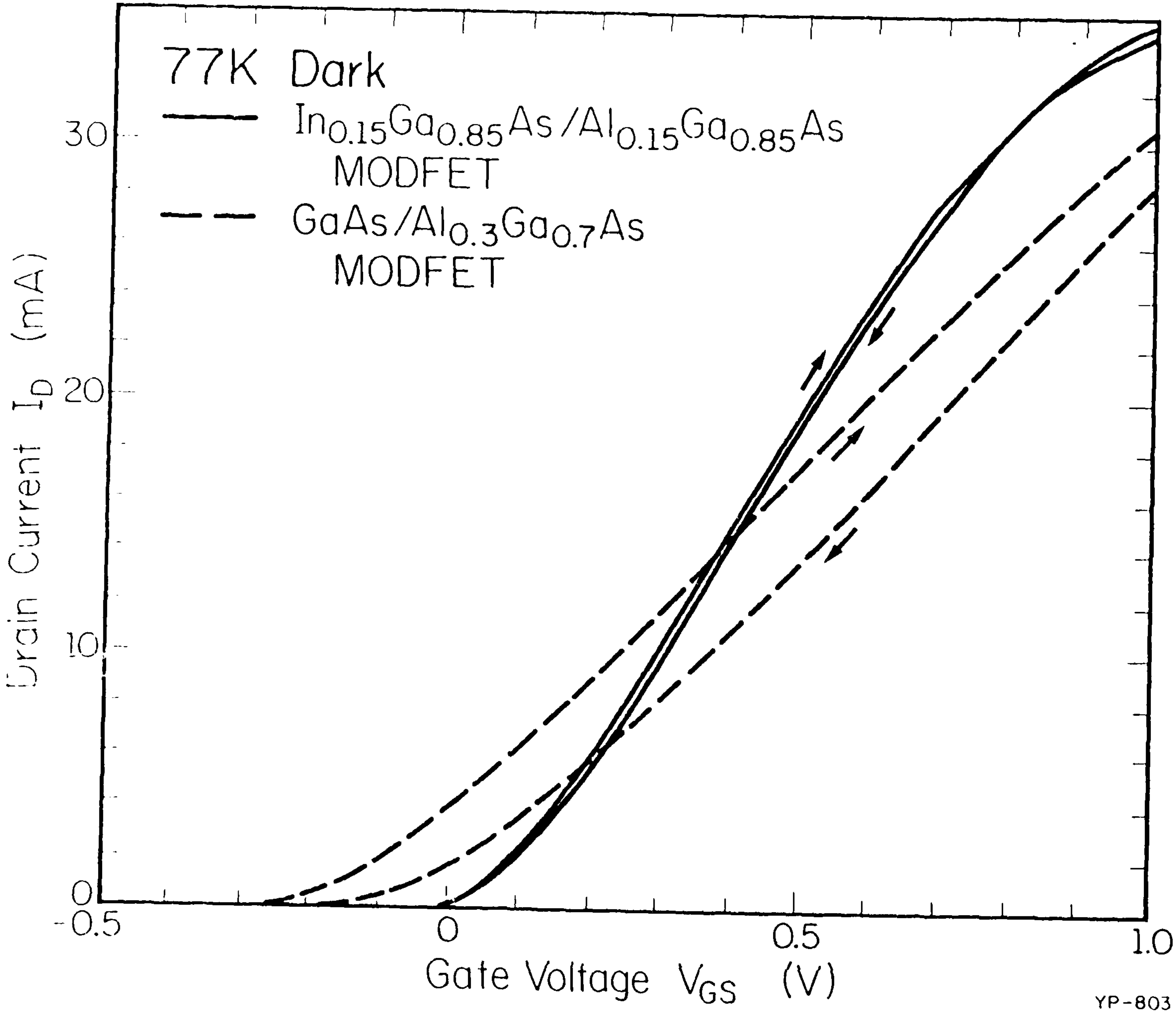


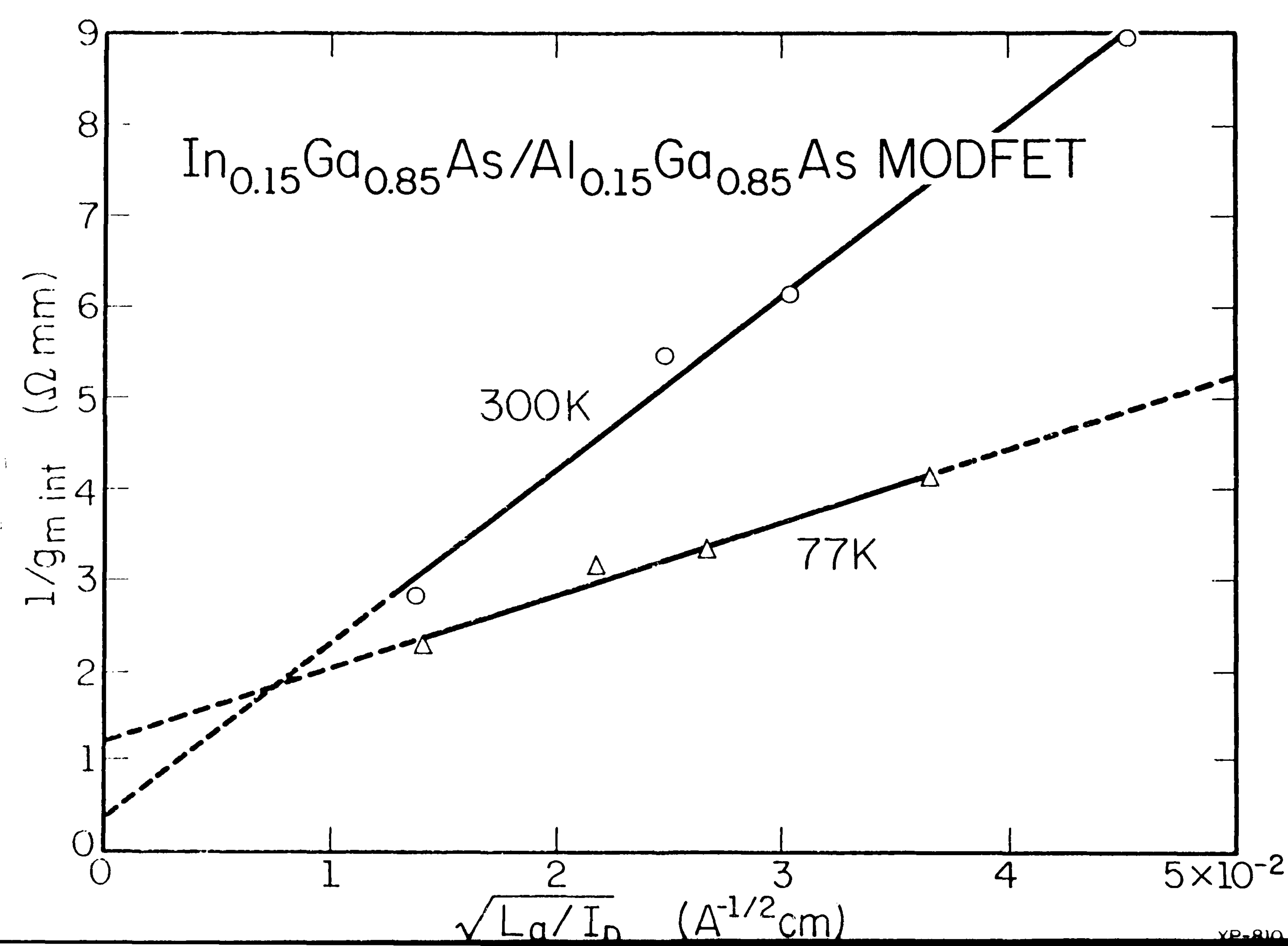
300K
Drain Current I_D (mA)
Transconductance g_m (mS/mm)
Gate Voltage V_{GS} (V)


77K Dark
Drain Current I_D (mA)
0
10
20
30
40
50
Drain Voltage V_{DS} (V)
0
1
2

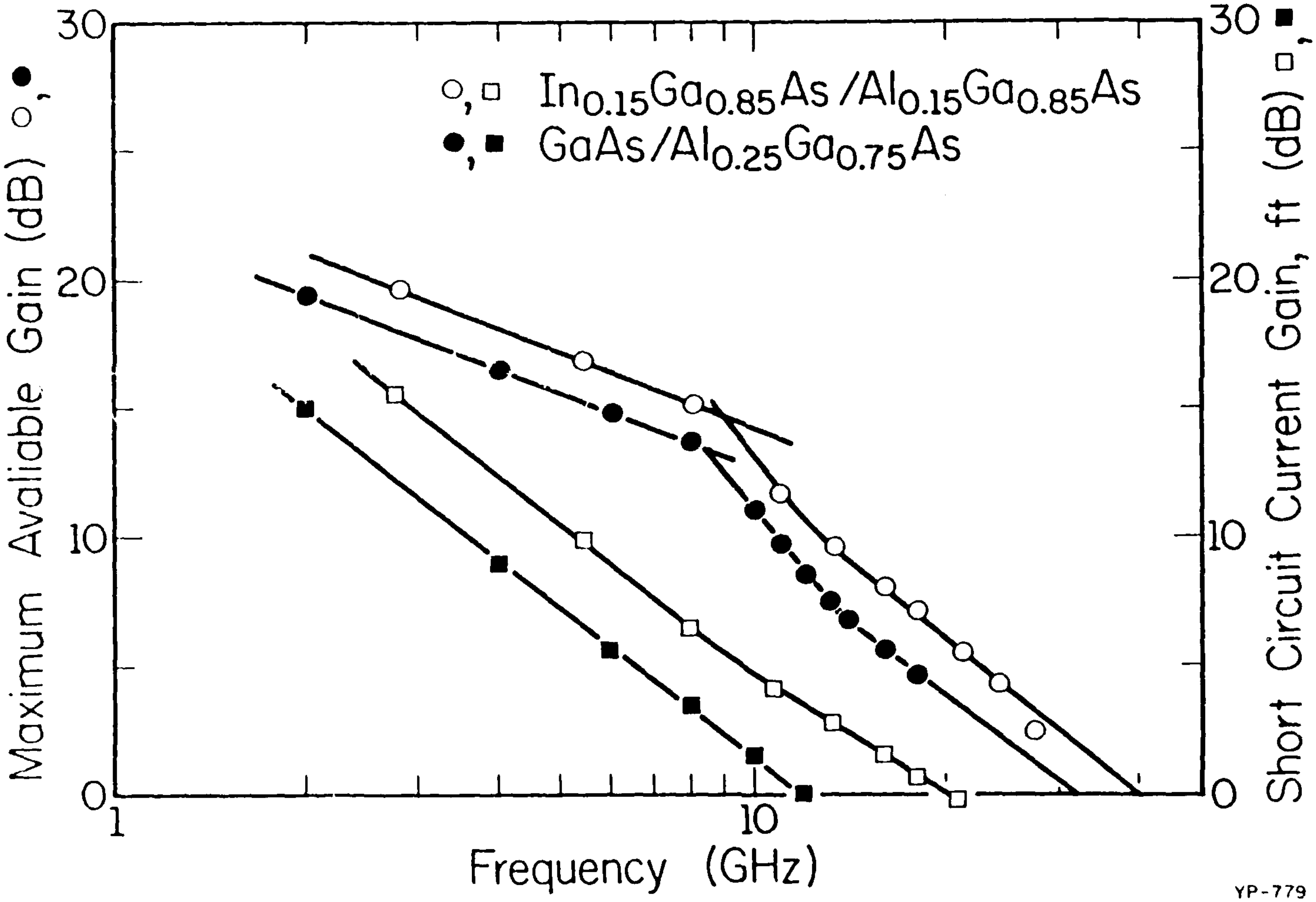
(a)


77K
Drain Current I_D (mA)
0
10
20
30
40
50
Transconductance g_m (mS/mm)
0
80
160
240
320
400
Gate Voltage V_{GS} (V)
-0.6
0
1.0

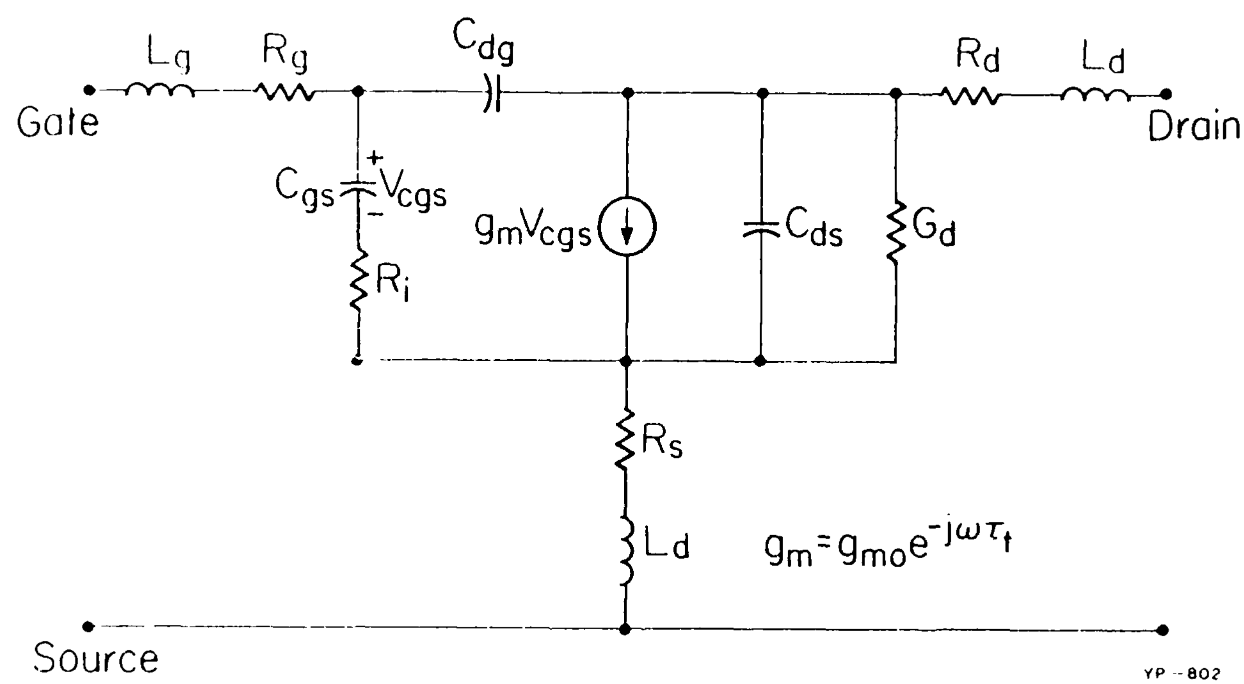

77K Dark
In0.15Ga0.85As/Al0.15Ga0.85As MODFET
GaAs/Al0.3Ga0.7As MODFET
Drain Current I_D (mA)
0
10
20
30
-0.5
0
0.5
1.0
Gate Voltage V_GS (V)
YP-803



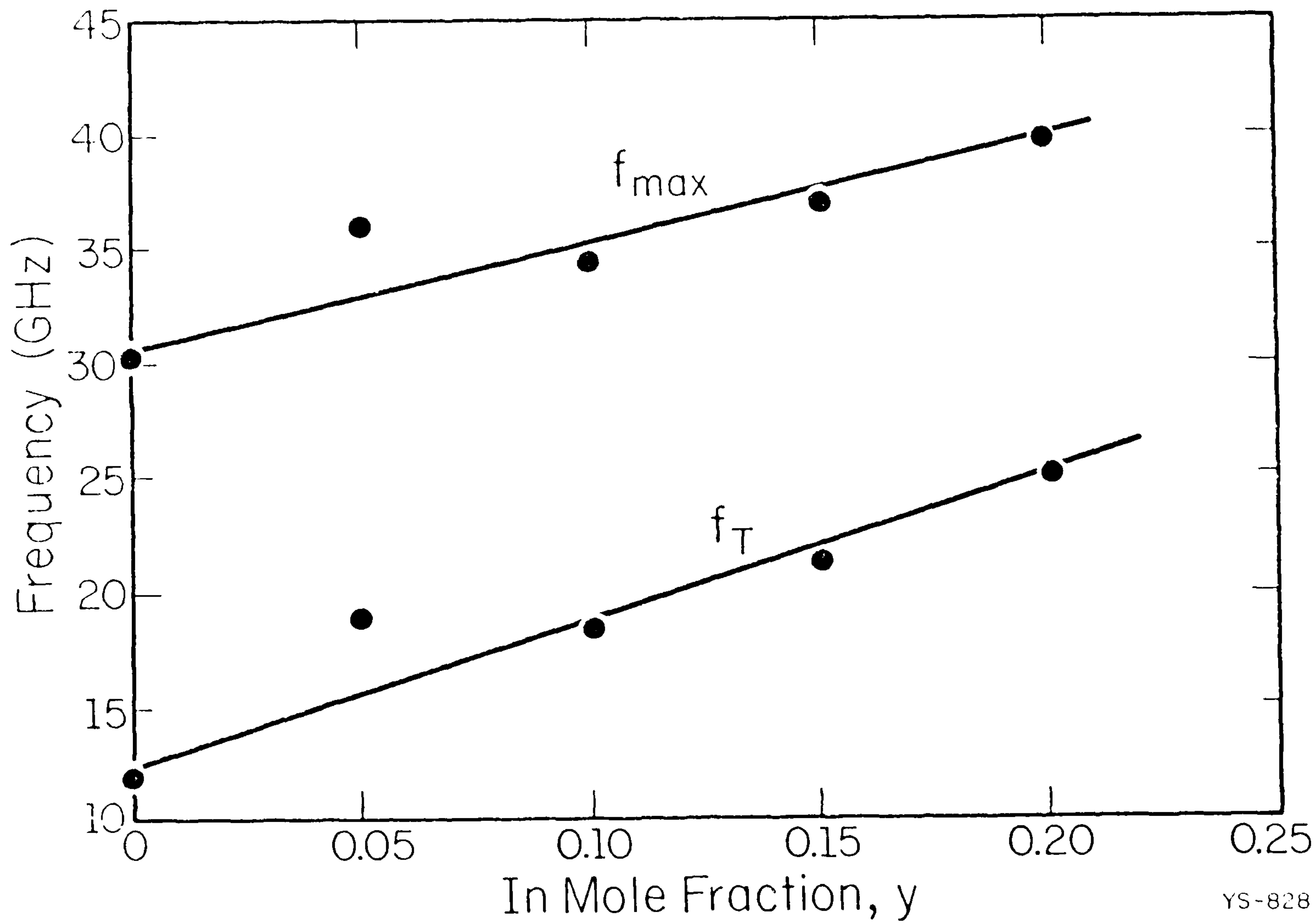
$In_{0.15}Ga_{0.85}As/Al_{0.15}Ga_{0.85}As$ MODFET
300K
77K
$1/g_{m\,int}$ (Ω mm)
$\sqrt{L_g/I_D}$ ($A^{-1/2}$cm)
0
1
2
3
4
5
6
7
8
9
5×10^{-2}


○, □ In0.15Ga0.85As / Al0.15Ga0.85As
●, ■ GaAs / Al0.25Ga0.75As
Maximum Available Gain (dB) ○, ●
Short Circuit Current Gain, ft (dB) □, ■
Frequency (GHz)
0
10
20
30
1
10

YP-779



Gate
Lg
Rg
Cdg
Rd
Ld
Drain
Cgs
+
Vcgs
−
Ri
gmVcgs
Cds
Gd
Rs
Ld
gm = gmoe-jωτt
Source
YP-802



45
40
35
30
25
20
15
10
Frequency (GHz)
f max
f T
0
0.05
0.10
0.15
0.20
0.25
In Mole Fraction, y

YS-828

InGaAs/InAlAs Hot Electron Transistor

The transport of hot electrons in thin semiconductor structures has been receiving a great deal of attention because of the possibility of collision free transport which in turn can lead to ultrafast devices. With crystal growth techniques such as molecular beam epitaxy (MBE) one can make devices whose dimensions are comparable to the carrier mean free paths. In such structures, the probability of electrons traversing the devices ballistically increases as their dimensions get smaller. Recently Heiblum et. al.[1] showed that about 50% of the electrons exhibit ballistic transport in a 300Å thick GaAs layer at liquid helium temperature. Various hot electron transistor (HET) structures have been used by several authors[2-5] to obtain the distribution of hot electrons at low temperatures. Although Shur and Eastman[6] proposed a purely ballistic model for electron transport in a diode structure composed of n^+-n^--n^+ layers, consideration of inherent problems in the device structures[7-8] made it hard to prove the ballistic effect. Double barrier resonant tunneling structure has also been used as an electron injector.[9] In this report we present results that indicate the existence of ballistic transport through a 0.3μm thick n-InGaAs plus 800Å thick InAlAs semiconductor layer at relatively high temperatures (77K).

The structure used in the present investigation (described in Fig. 1) was grown by molecular beam epitaxy on an InP substrate. The substrate was held at 510°C and the n-type dopant was Si. A three terminal device was formed using two i-$In_xAl_{1-x}As$ barriers. This resembles a unipolar transistor and the usual convention was adopted to describe the currents and voltages. The emitter-base junction which functions as the hot electron injector was formed by placing a 75Å thin i-$In_xAl_{1-x}As$ (x=0.52) barrier between two n^+ InGaAs

layers, both doped to $5x10^{17}cm^{-3}$. The base-collector junction was formed by placing a 800Å i-$In_xAl_{1-x}As$ (x=0.52) barrier between two n^+ $In_yGa_{1-y}As$ (y=0.53), layers. The above compositions were chosen to lattice match the layers and thus reduce electron scattering. The common 0.3μm thick n^+ $In_yGa_{1-y}As$ (y=0.53) layer was the base and formed the transit region for the injected hot electrons. The collector was doped to $2x10^{18}cm^{-3}$.

The energy band diagram of the device is shown schematically in Fig. 1. The potential barrier height due to band discontinuity between $In_yGa_{1-y}As$ and $In_xAl_{1-x}As$ is about 0.6eV. Biasing the emitter negative with respect to the base causes electrons to tunnel through the emitter barrier and reach the base region with energies close to eV_{BE}. Since the electron mean free path in InGaAs is large compared to that in GaAs we were able to make the base region relatively thick (3000Å).

By cooling the device, thermal currents are reduced and tunneling currents enhanced. The device characteristics measured at 77K are shown in Fig. 2. The collector current I_C for different emitter currents I_E ranging from 2.0 mA to 3.5 mA is plotted as a function of V_{CB}. In the absence of electron injection from the emitter (I_E=0) Fowler-Nordheim tunneling of base electrons form the collector current.

Application of a negative emitter base voltage raises the electron energy and when the Fermi level in the emitter reaches the triangular part of the emitter-base barrier, Fowler-Nordheim tunneling of electrons occur. Due to the large band discontinuity between InGaAs and InAlAs and the voltage drop across the base resistance, considerable emitter-base voltages (>0.7v) are required. The electron energy as they are injected into the base is about 700 meV. About 1.6% of these electrons are collected at the collector which are

ballistic. The average mean free path, considering transport through InGaAs base and InAlAs barrier, calculated from this figure is 920Å. This apparently small figure is a result of our particular device structure: the large emitter barrier, thick base region and thick collector barrier contribute to the small gain. In addition, the injected hot electrons see an abrupt collector barrier resulting in appreciable quantum mechanical reflections.

In Fig. 3 the conductance, defined as the derivative of I_C with respect to V'_{CB} is plotted for different I_E. The conductance is proportional to the number of electrons as a function of electron energy,[2] $\frac{dI_C}{dV'_{CB}} \propto n(E_n)$ for negative collector voltages. In this region collector current I_C slowly decreases and rapidly drops to zero below a threshold voltage which increases with V'_{BE}. It is clear from the figure that the main ballistic peak shifts to larger negative voltages as the energy of the injected hot electrons increases. This shift in the peak towards more negative V'_{CB} is larger than the voltage drop across the 20Ω base resistance confirming ballistic transport. The full width at half maximum remains constant at about 130 meV. While this may seem large compared to values obtained for a 300Å thick base as reported in Ref. 1, when viewed in terms of the large emitter voltages needed for tunneling in the emitter barrier, and the thick base region, the observed width seems reasonable. The non-abrupt drop to zero in collector current observed near the threshold voltage is indicative of this fact. The tail on the left side of the peak, we believe is the result of some injected electrons tunneling through the top of the triangular collector barrier.

In Table I we present the results obtained in our investigation. It is assumed that the electrons have the same energy before and after tunneling through the emitter barrier. Thus the maximum energy of the tunneling

electrons eV'_{BE} is given by

$$eV'_{BE} = \phi - \eta + e|V'_{CB}| \tag{1}$$

where ϕ = Collector barrier height

η = Height of Fermi level above the conduction band in the collector.

V'_{CB} = Collector voltage corresponding to maximum electron energy.

The calculated energies of the $In_xAl_{1-x}As$ barrier are given in the last column. The values range from 600 meV to 678 meV with an average of 633.6 meV. This is in reasonable agreement with the barrier height of 0.6 eV obtained by thermionic emission measurements. The observed spread of about 35 meV in our experiment, we believe, is due to the dispersion of tunneling electrons in the thick base region.

In summary, we have observed ballistic transfer of electrons at 77K in a relatively thick (0.3μm) $In_{0.53}Ga_{0.47}As$ layer forming the base of a hot electron transistor. The low ballistic gains (1.6%) observed are explained in terms of the large transit region and the high collector and emitter barriers used.

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Figure Captions

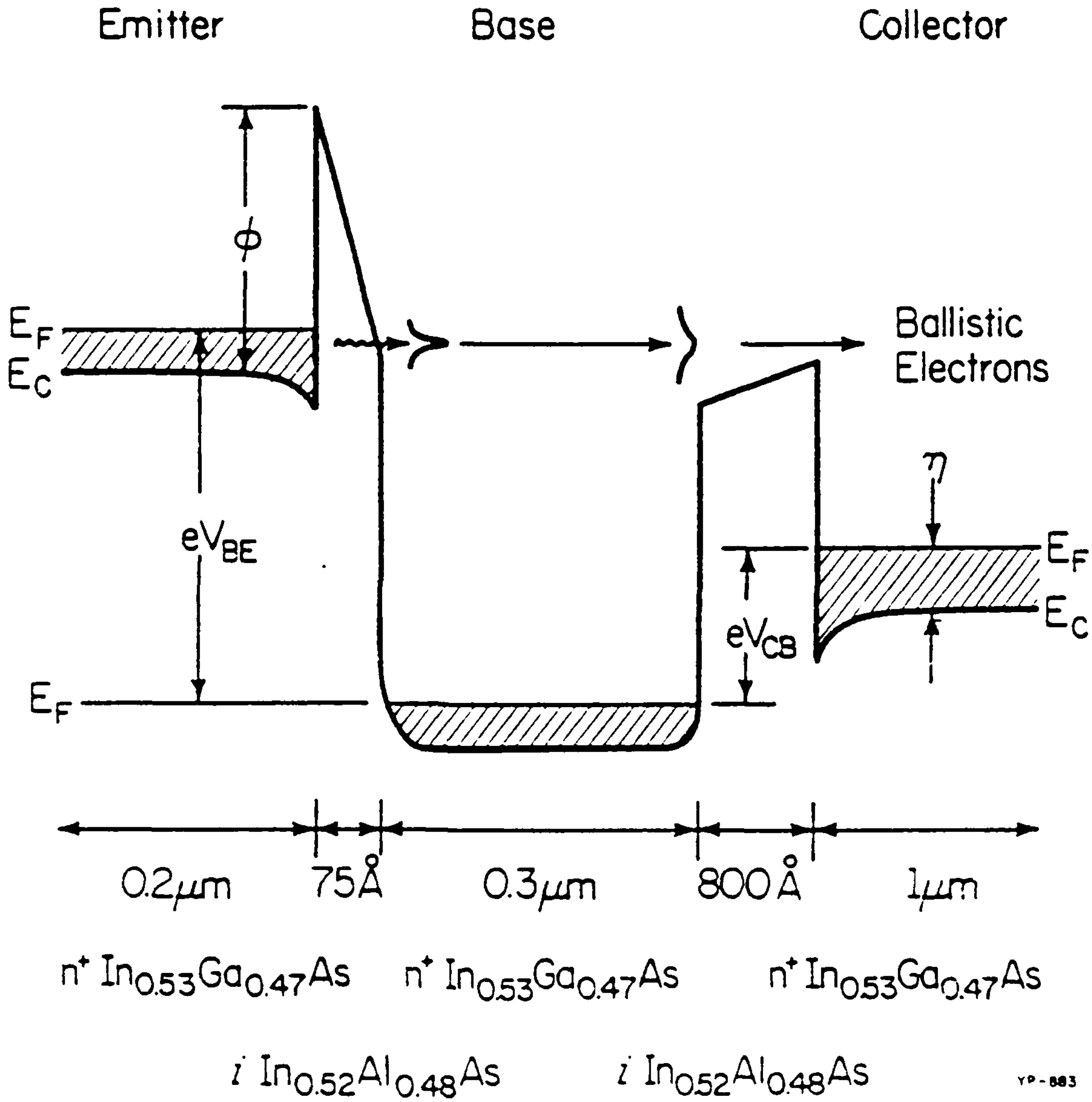
Fig. 1. Energy band diagram of the hot electron spectrometer. V_{BE}, V_{CB} are the emitter and collector voltage with the base region grounded. ϕ is the $In_xAl_{1-x}As$ barrier height, η- the height of the collector Fermi level above the conduction band.

Fig. 2. Variation of collector current with V'_{CB}, for different emitter currents I_E at 77K.

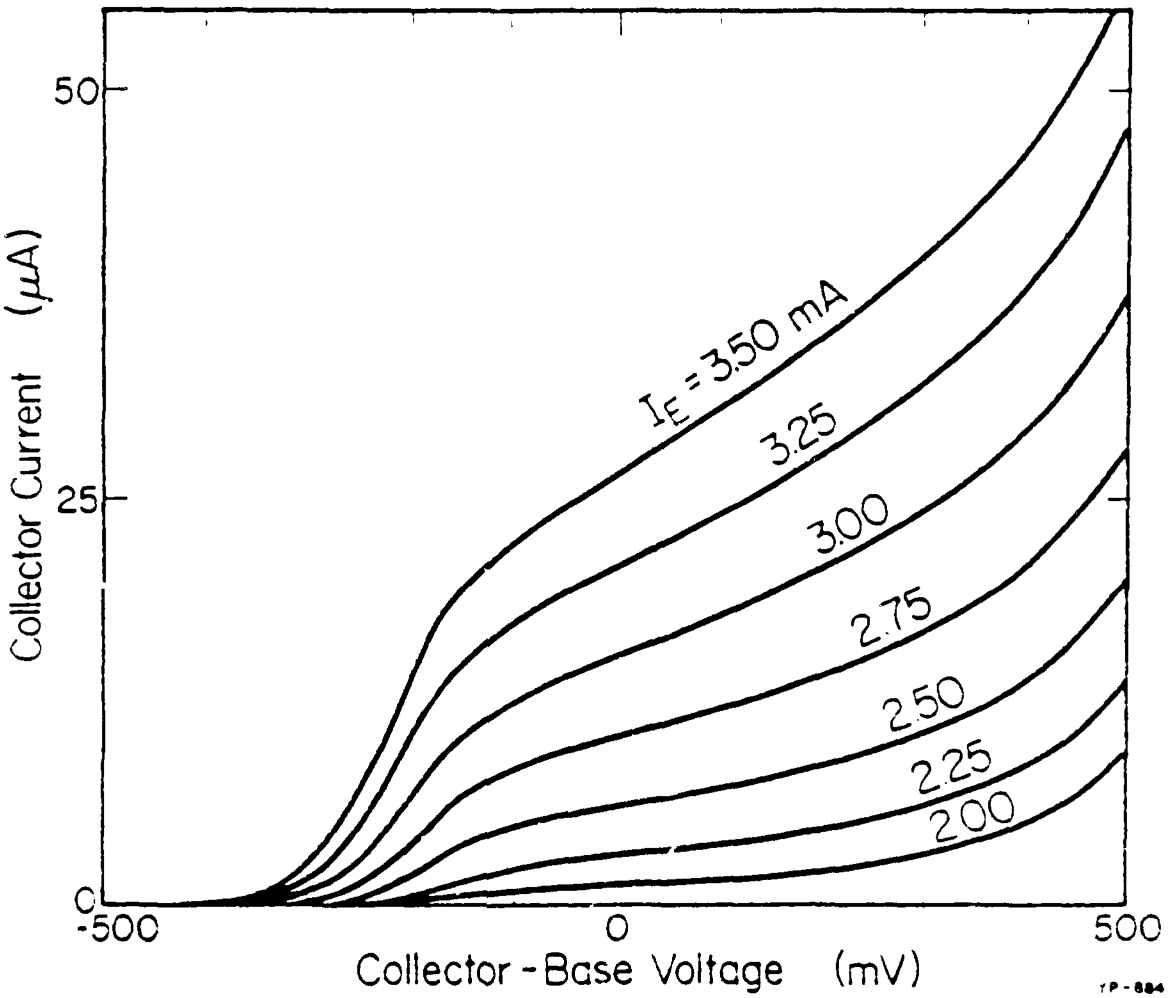
Fig. 3. Plot of conductance as a function of V'_{CB} for different I_E at 77K, showing the ballistic peak.

Table I

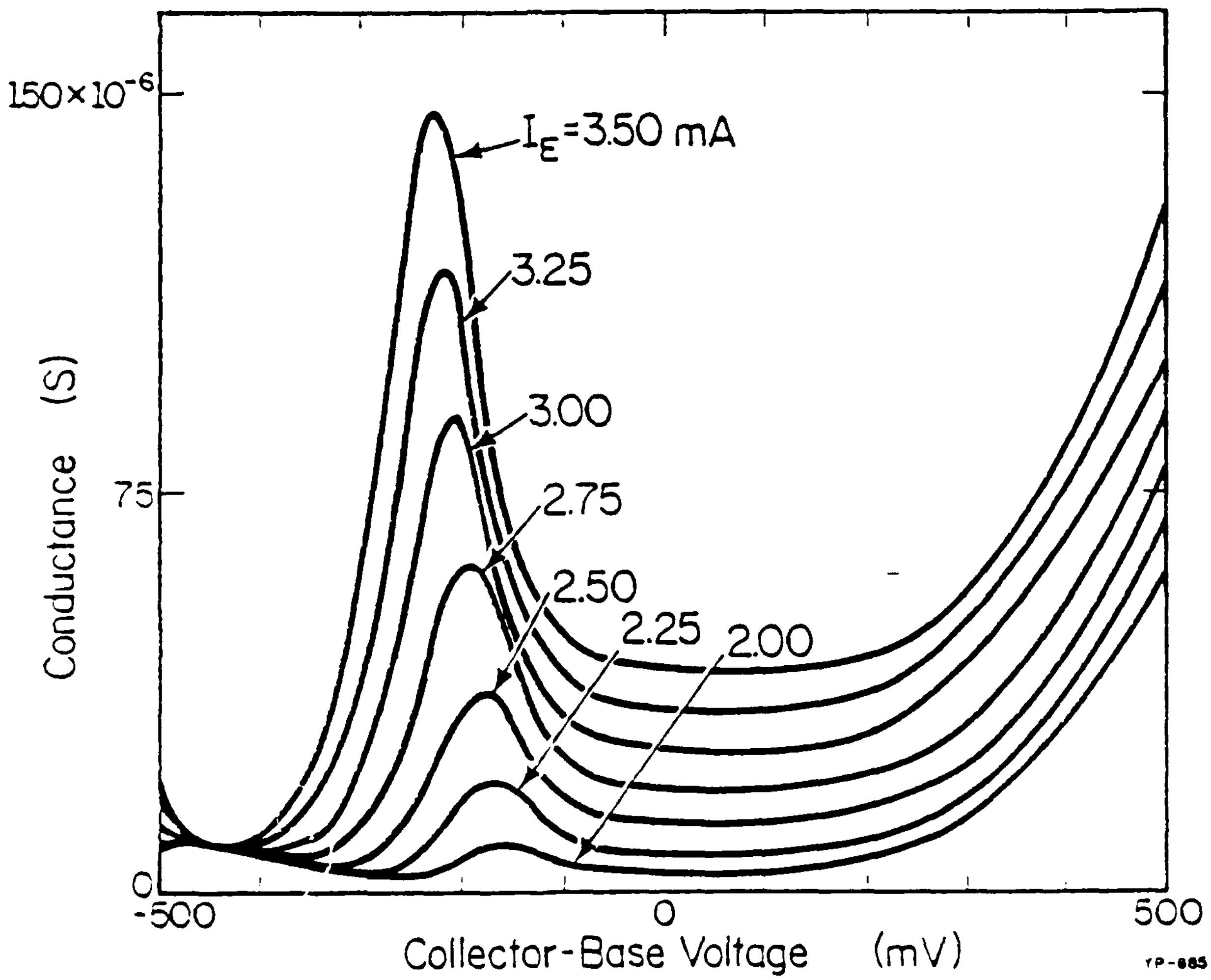
I_E (mA)	V_{BE} (mV)	$\lvert V_{CB}' \rvert$ (mV)	$\emptyset$ (meV)
2.50	650	179	600
2.75	682	190	621
3.00	718	202	645
3.25	747	214	662
3.50	779	230	678
			Av. 633.6



Emitter
Base
Collector
ϕ
E_F
E_C
Ballistic Electrons
η
eV_{BE}
E_F
E_C
eV_{CB}
E_F
0.2μm
75Å
0.3μm
800 Å
1μm
$n^+ In_{0.53}Ga_{0.47}As$
$n^+ In_{0.53}Ga_{0.47}As$
$n^+ In_{0.53}Ga_{0.47}As$
$i\ In_{0.52}Al_{0.48}As$
$i\ In_{0.52}Al_{0.48}As$
YP-883



50
25
0
-500
0
500
Collector Current (μA)
Collector - Base Voltage (mV)
I_E = 3.50 mA
3.25
3.00
2.75
2.50
2.25
2.00
TP-884



150×10⁻⁶
75
0
Conductance (S)
-500
0
500
Collector-Base Voltage (mV)
I_E=3.50 mA
3.25
3.00
2.75
2.50
2.25
2.00
YP-885

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